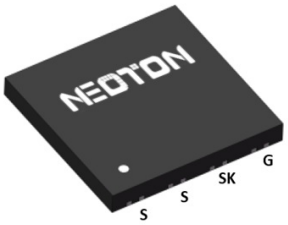
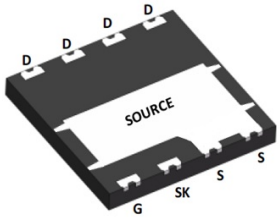
Description

The device is a N-channel 650 V power transistor based on proprietary Enhancement-mode (E-mode) GaN on silicon technology. The inherent advantages of this device over silicon MOSFETs include extremely low on-state resistance, ultra-low input and output capacitance, and zero reverse-recovery charge, making it suitable for applications that require superior power density, ultra-high switching frequency, and outstanding efficiency.

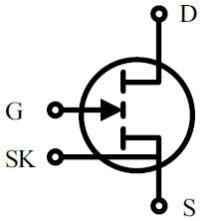




Features

- E-mode power transistor – Normally OFF switch
- Higher operating frequency than Si or SiC based transistors
- Zero reverse-recovery charge
- Reverse conduction capability
- Low gate charge, and low output charge
- High system efficiency and power density
- Qualified for standard grade applications according to JEDEC Standards

Gate	4
Drain	5,6,7,8
Kelvin Source	3
Source	1,2



Applications

- Consumer and industrial switching power supplies
- Power factor correction
- Power adapters
- Fast battery charging
- High density and efficiency power conversion

Ordering Code	Package	Marking
NT1H110065S1	DFN 8X8	1H110065

Key performance parameters (at T_J = 25°C)

Parameter	Value	Unit
$V_{DS,max}$	650	V
$R_{DS(ON)}$ @ V_{GS} = 6V	100	mΩ
$Q_{G,typ}$ @ V_{DS} = 400V	7.7	nC
$I_{D,pulse}$	32	A
Q_{OSS} @ V_{DS} = 400V	33	nC
Q_{rr} @ V_{DS} = 400V	0	nC

Absolute Maximum Ratings (at T_J = 25°C unless otherwise specified)

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain to source voltage	$V_{DS, max}$	650	V	V_{GS} = 0 V; T_J = -55 °C to 150 °C
Drain to source voltage, transient	$V_{DS, transient}$	800	V	V_{GS} = 0 V; t_{PULSE} < 200 µs
Gate to source voltage, continuous	V_{GS}	-10 to +7	V	T_J = -55 °C to 150 °C
Continuous drain current	I_D	18	A	T_C = 25 °C
Pulsed drain current	$I_{D, pulse}$	32	A	T_C = 25 °C; V_{GS} = 6 V; t_{PULSE} = 300 µs
Pulsed drain current	$I_{D, pulse}$	20	A	T_C = 125 °C; V_{GS} = 6 V; t_{PULSE} = 300 µs
Power dissipation	P_{tot}	128	W	T_C = 25 °C
Operating junction temperature	T_J	-55 to +150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

Thermal Characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction-to-ambient	$R_{\Theta JA}$	53	°C/W	FR-4 substrate PCB 2 oz copper 1” square pad layout
Thermal resistance, junction-to-case	$R_{\Theta JC}$	0.98	°C/W	
Maximum soldering temperature	T_{sold}	260	°C	MSL3

Electrical Characteristics (at T_J = 25 °C unless otherwise specified)

Static Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain-source on-state resistance	$R_{DS(on)}$		100	138	mΩ	V_{GS} = 6 V; I_D = 5 A; T_J = 25 °C
			228			V_{GS} = 6 V; I_D = 5 A; T_J = 150 °C
Gate threshold voltage	$V_{GS(th)}$		1.4		V	I_D = 9 mA; V_{DS} = V_{GS}; T_J = 25 °C
			1.5			I_D = 9 mA; V_{DS} = V_{GS}; T_J = 150 °C
Drain-source leakage current	I_{DSS}		3		μA	V_{DS} = 650 V; V_{GS} = 0 V; T_J = 25 °C
			50			V_{DS} = 650 V; V_{GS} = 0 V; T_J = 150 °C
Gate-source leakage current	I_{GSS}		462		μA	V_{GS} = 6 V; V_{DS} = 0 V
Gate resistance	R_G		3.9		Ω	f = 5 MHz; open drain

Dynamic Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{ISS}		116		pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Output capacitance	C_{OSS}		48		pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Reverse transfer capacitance	C_{RSS}		2.1		pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related	$C_{O(ER)}$		70		pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related	$C_{O(TR)}$		83		pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}		33		nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Turn-on delay time	$t_{D(on)}$		2.7		ns	V_{DS} = 400 V; I_D = 10 A; L = 100 μH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 2 Ω; See Figure 19;20
Turn-off delay time	$t_{D(off)}$		7.4		ns	
Rise time	t_R		9.4		ns	
Fall time	t_F		4.0		ns	
Switching energy during turn-on	E_{on}		28		μJ	
Switching energy during turn-off	E_{off}		2.6		μJ	
Output capacitance stored energy	E_{OSS}		5.6		μJ	V_{DS} = 400 V V_{GS} = 0 V; f = 100 kHz

Gate Charge Characteristics

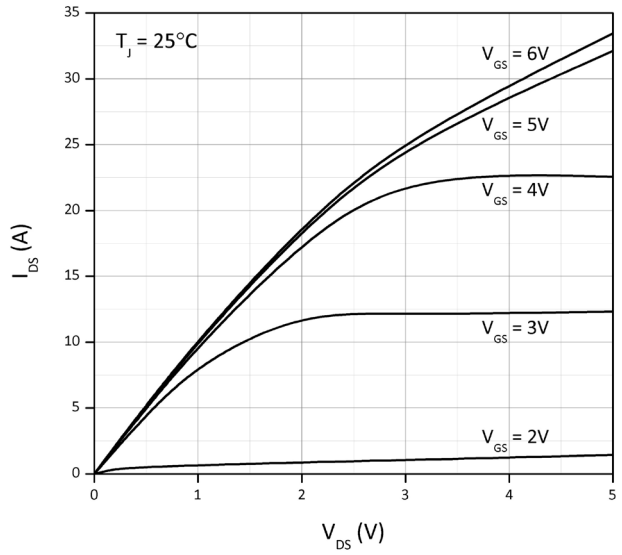
Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Total gate charge	Q_G		7.7		nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_{DS} = 5 A
Gate-source charge	Q_{GS}		1.3		nC	
Gate-drain charge	Q_{GD}		2.7		nC	
Gate plateau voltage	V_{Plat}		2.4		V	V_{DS} = 400 V; I_{DS} = 5 A

Reverse Conduction Characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}		2.3		V	V_{GS} = 0 V; I_{SD} = 5 A
Pulsed current, reverse	$I_{S,\ pulse}$			32	A	V_{GS} = 6 V; t_{PULSE} =300 µs
Reverse recovery charge	Q_{rr}		0		nC	I_{SD} = 5 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}		0		ns	
Peak reverse recovery current	I_{rrm}		0		A	

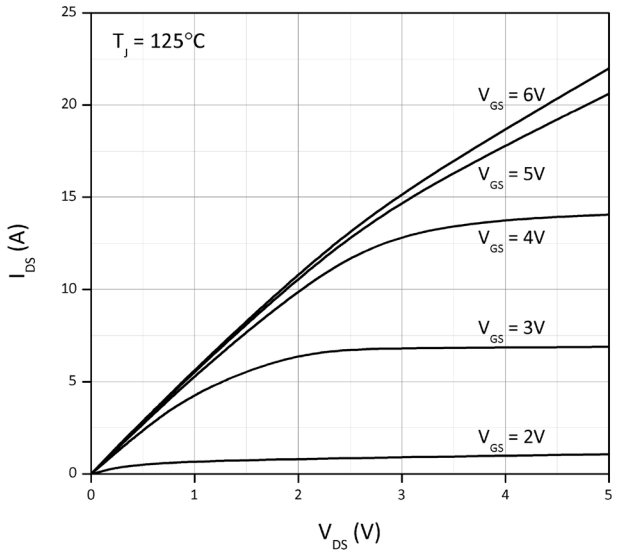
Electrical Performance Diagrams (at T_J = 25 °C unless otherwise specified)

Figure 1 : Typical output characteristics



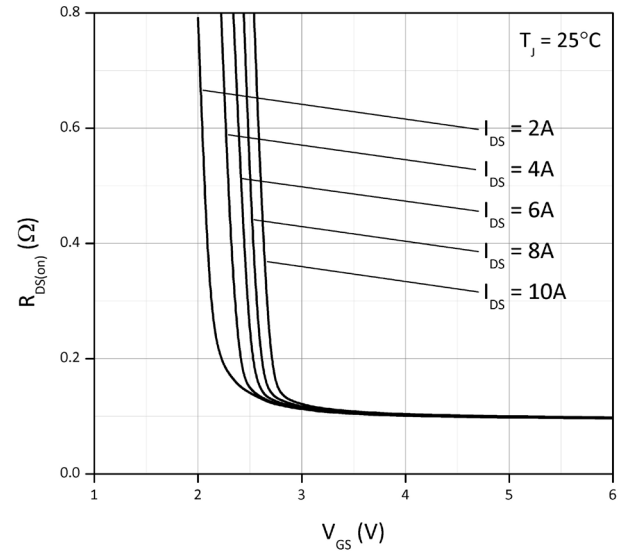
I_{DS} = f(V_{DS}, V_{GS}); T_J = 25°C

Figure 2 : Typical output characteristics



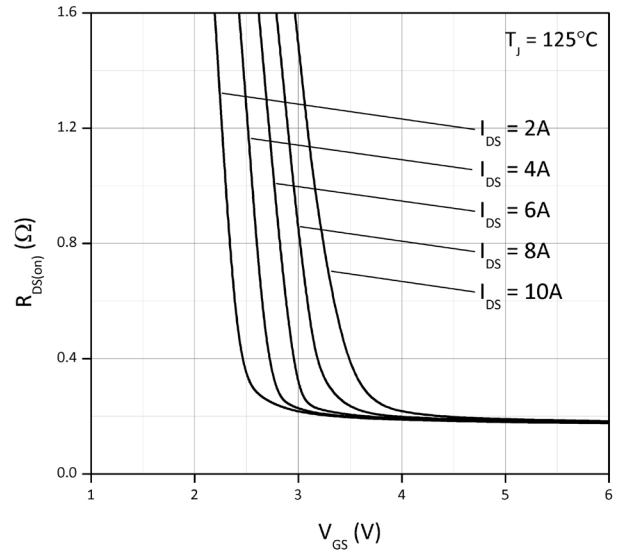
I_{DS} = f(V_{DS}, V_{GS}); T_J = 125°C

Figure 3 : Typical drain-source on resistance



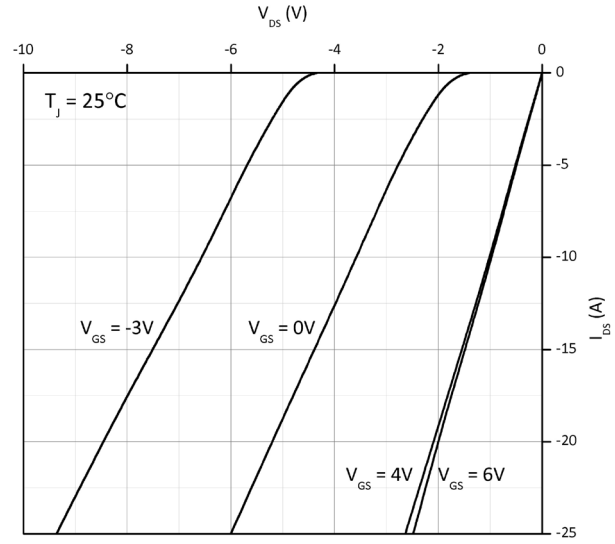
$R_{DS(ON)}$ = f(I_{DS}, V_{GS}); T_J = 25°C

Figure 4 : Typical drain-source on resistance



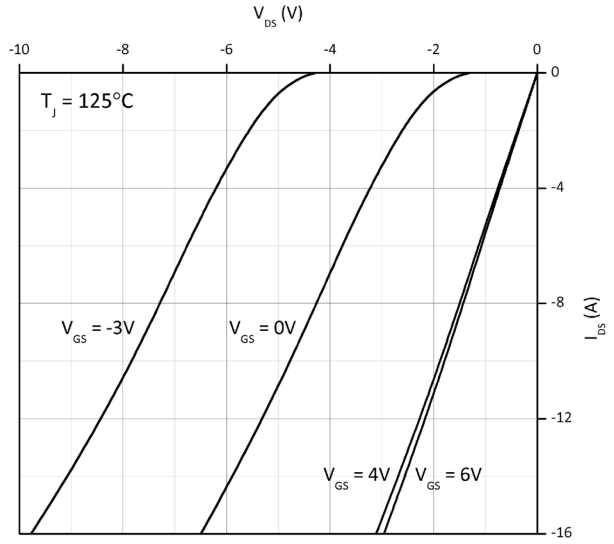
$R_{DS(ON)}$ = f(I_{DS}, V_{GS}); T_J = 125°C

Figure 5 : Typical channel reverse characteristics



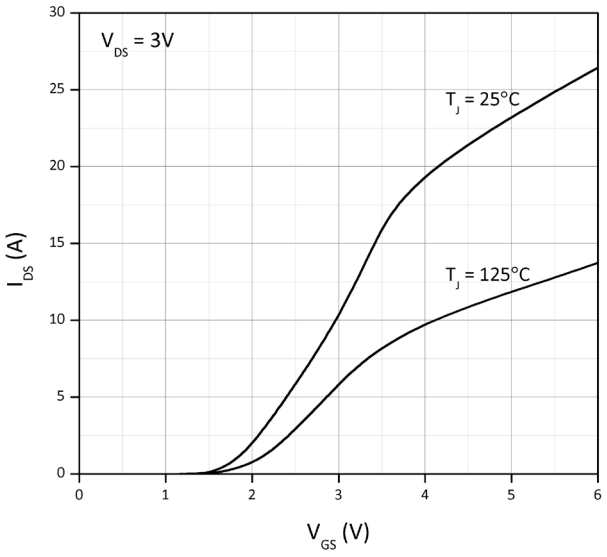
$I_{DS} = f(V_{DS}, V_{GS})$; $T_J = 25°C$

Figure 6 : Typical channel reverse characteristics



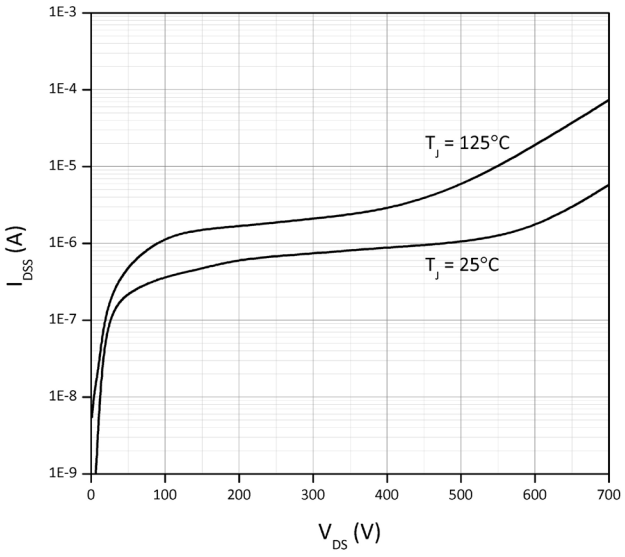
$I_{DS} = f(V_{DS}, V_{GS})$; $T_J = 125°C$

Figure 7 : Typical transfer characteristics



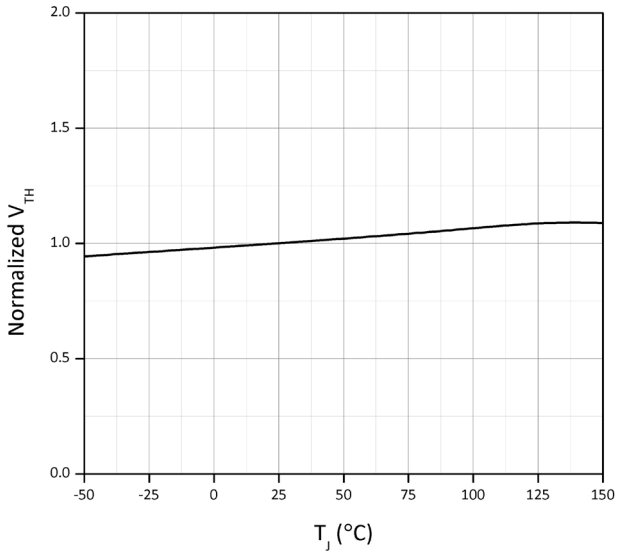
$I_{DS} = f(V_{GS})$; $V_{DS} = 3$ V

Figure 8 : Typical drain-source leakage



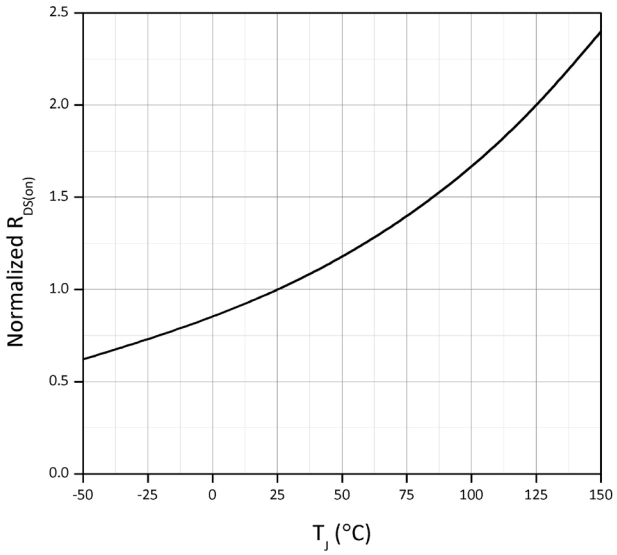
$I_{DSS} = f(V_{DS})$; $V_{GS} = 0$ V

Figure 9 : Gate threshold voltage



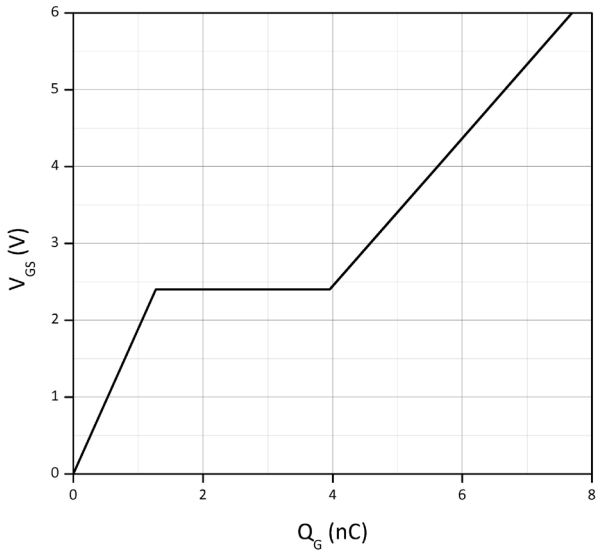
$V_{GS(TH)} = f(T_J)$; $V_{GS} = V_{DS}$; I_{DS} = 9 mA

Figure 10 : Drain-source on-state resistance



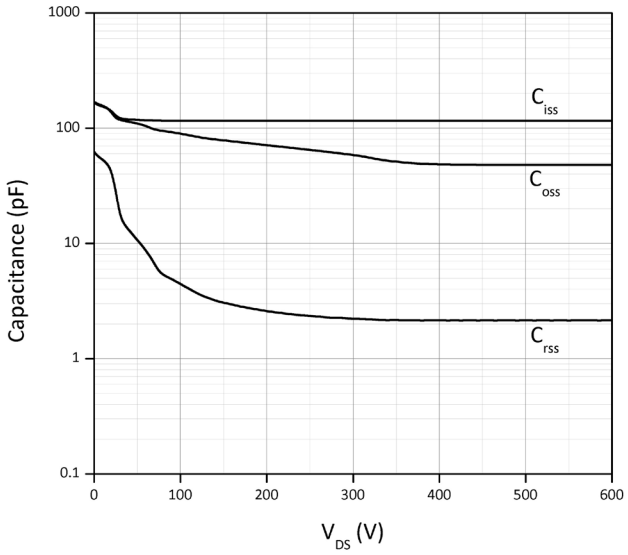
$R_{DS(ON)} = f(T_J)$; V_{GS} = 6 V; I_{DS} = 5 A

Figure 11 : Typical gate charge



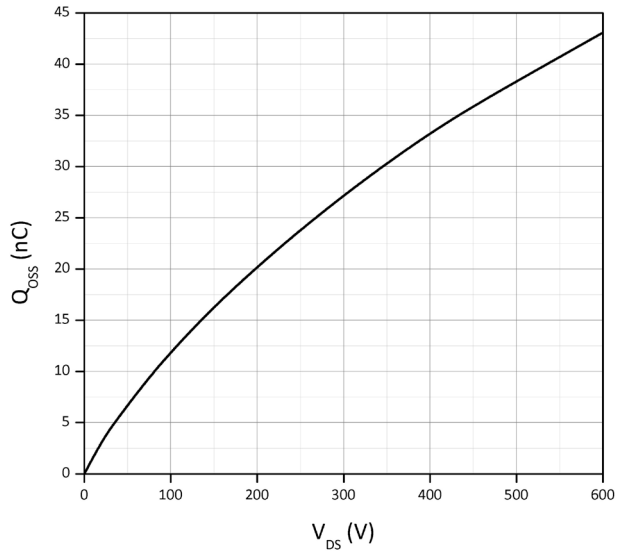
$V_{GS} = f(Q_G)$; V_{DS} = 400 V; I_{DS} = 5 A

Figure 12 : Typical capacitances



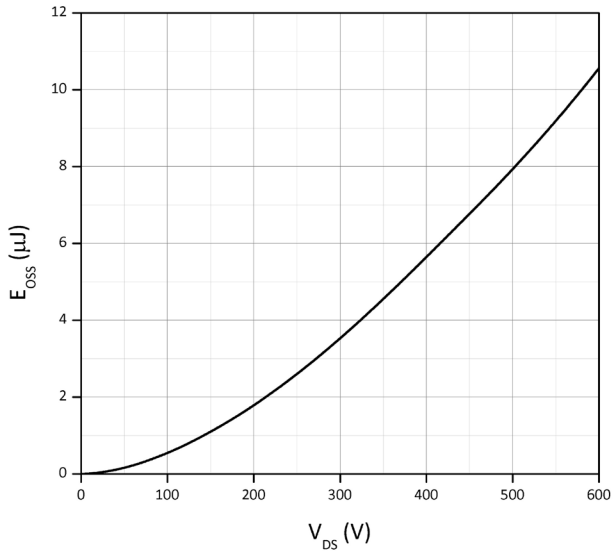
C = f(V_{DS}); freq. = 100 kHz

Figure 13 : Typical output charge



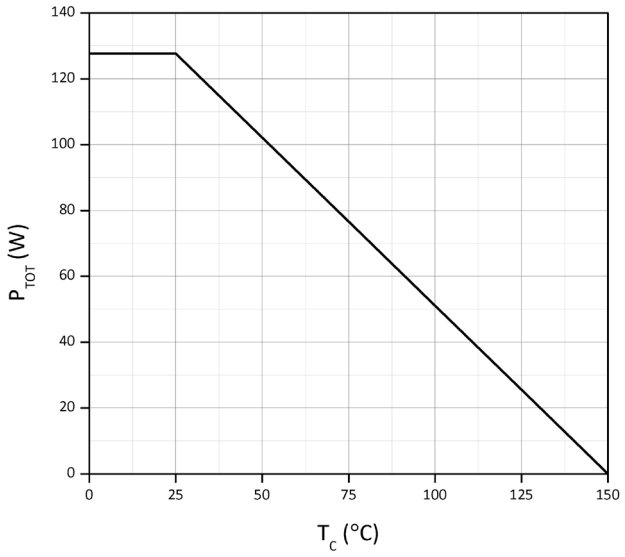
Q_{OSS} = f(V_{DS}); freq. = 100 kHz

Figure 14 : Typical C_{OSS} stored energy



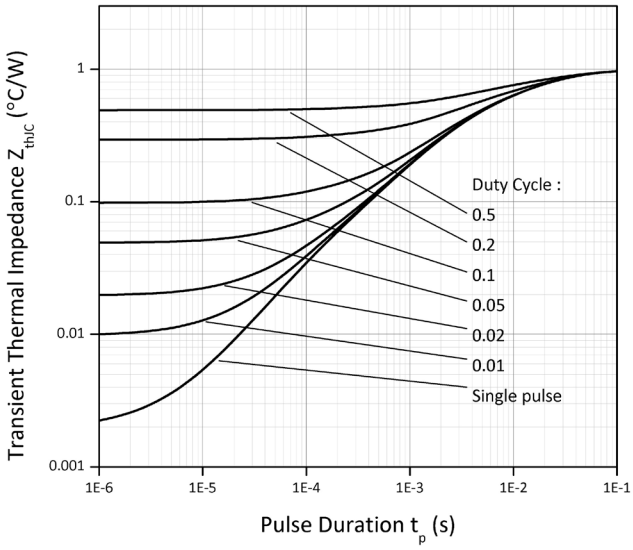
E_{OSS} = f(V_{DS}); freq. = 100 kHz

Figure 15 : Total power dissipation



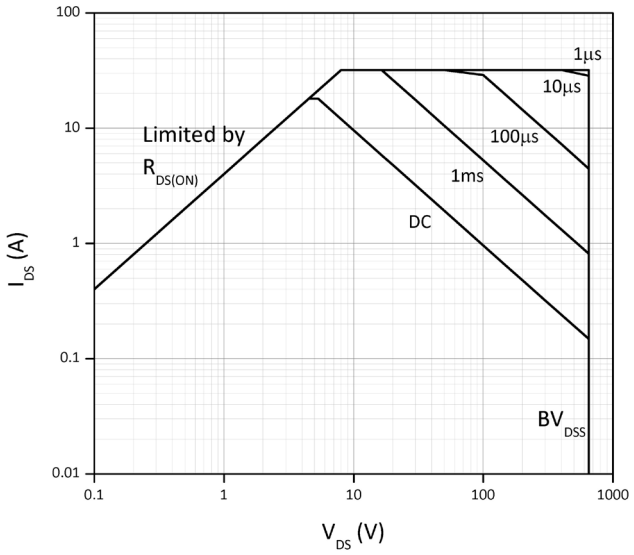
P_{TOT} = f(T_C)

Figure 16 : Transient thermal impedance



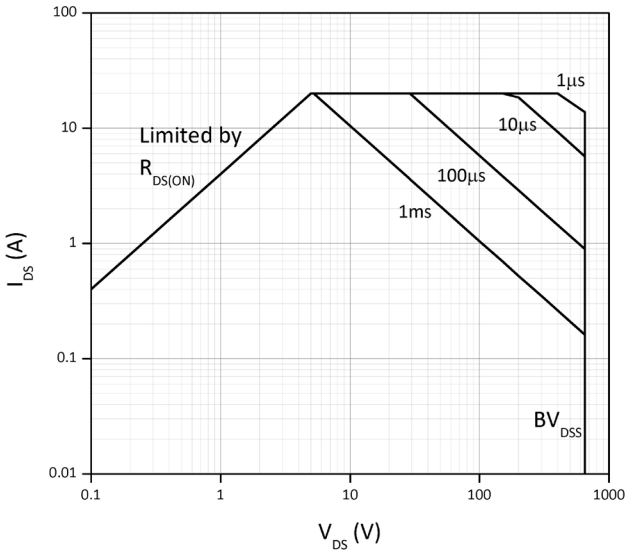
Z_{thJC} = f(t_P, D)

Figure 17 : Safe operating area



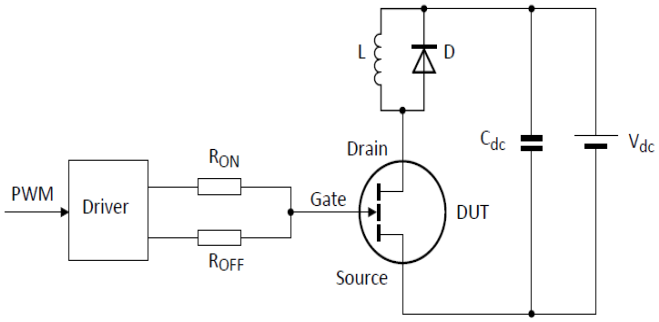
$I_{DS} = f(V_{DS})$; $T_C = 25°C$

Figure 18 : Safe operating area



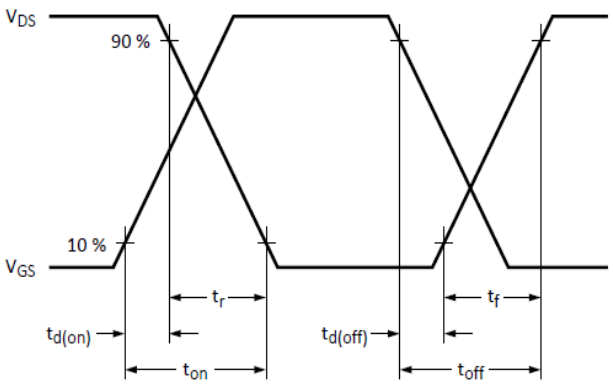
$I_{DS} = f(V_{DS})$; $T_C = 125°C$

Figure 19 : Switching times with inductive load

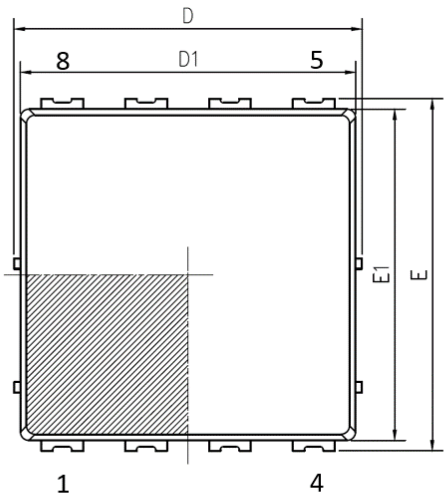


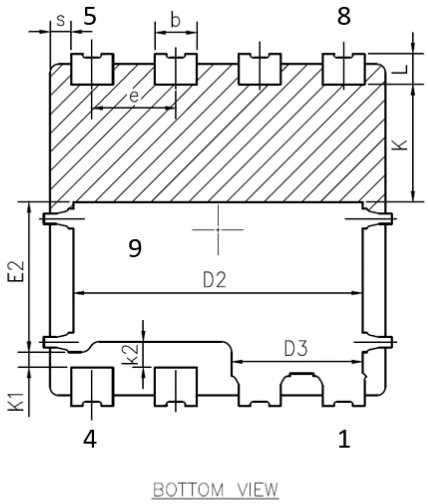
V_{DS} = 400 V, I_{DS} = 10 A, L = 100 µH, V_{GS} = 6 V,
R_{on} = 10 Ω, R_{off} = 2 Ω

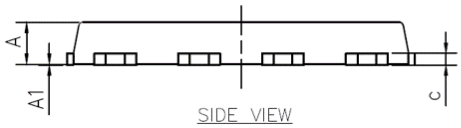
Figure 20 : Switching times waveform



Package Outlines

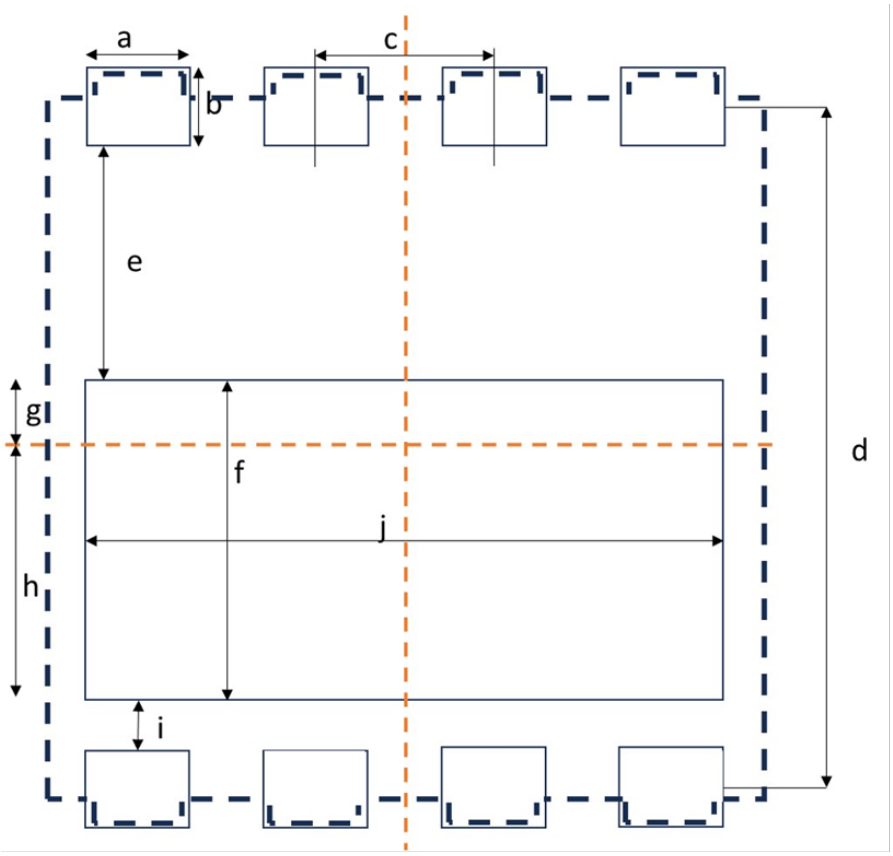






SYMBOL	DIMENSION (mm)			SYMBOL	DIMENSION (mm)		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	0.90	1.00	1.10	E1	7.80	7.90	8.00
A1	0.00		0.05	E2	3.48	3.58	3.68
b	0.90	1.00	1.10	e	2.00 BSC		
c	0.254			K	2.80 REF		
D	8.20	8.30	8.40	K1	0.36 REF		
D1	7.90	8.00	8.10	K2	0.61 REF		
D2	6.80	6.90	7.00	L	0.67	0.77	0.87
D3	3.02	3.12	3.22	S	0.45	0.50	0.55
E	8.30	8.40	8.50				

Recommended Footprint Outlines



SYMBOL	a	b	c	d	e	f	g	h	i	j
DIMENSION(mm)	1.20	1.00	2.00	7.65	2.60	3.50	0.70	2.80	0.55	7.30